REMARKS

Applicant respectfully requests consideration of the subject application.

Office Rejection Summary

Claims 1, 8, and 9 have been rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent 6,690,655 to Mark Miner et al. (hereinafter "Miner").

Claims 2-5 and 7 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Miner in view of Martin S. Michael (hereinafter "Michael").

Claim 6 has been rejected under 35 U.S.C. §103(a) as being unpatentable over Miner in view of Michael and further in view of Applicant's Admitted Prior Art (hereinafter "AAPA").

Claims 10-11 and 16-20 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Miner in view of U.S. Patent 6,429,706 to Dilip Amin et al. (hereinafter "Amin").

Claims 12-14 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Miner in view of U.S. Patent 6,163,823 to Gregory Henrikson (hereinafter "Henrikson").

Claim 15 has been rejected under 35 U.S.C. §103(a) as being unpatentable over Miner in view of Henrikson as applied to claim 12 of the Application and further in view of Michael.

Status Of Claims

Claims 1-20 remain pending in the application. Claims 1, 8, 12 and 16 have been amended to include pre-existing claim limitations. The amended claims are supported by the specification and no new matter has been added. No claim has been canceled.

Claim Rejections - §102(e)

Claims 1, 8, 9 have been rejected under §102(e) as being anticipated by Miner.

Amended independent claim 1 provides:

> A computer peripheral device comprising:
>
> a memory for storing a configuration address; and
>
> ***an independent*** power level control circuit for controlling the power level in the device so as to be in a standby mode or normal power mode after power is applied to the device, the circuit being coupled to the memory to ***control an initial assignment of*** configuration address from a bus ***to the memory*** when the ***circuit*** enters the normal power mode ***after it is activated by a software application.***. (emphasis added).

Amended independent claim 8 provides:

> A computer system comprising:
> a processor; and
>
> a plurality of peripheral devices coupled to the processor through at least one bus, each device having an independent power level control circuit for controlling the power level in the device to be in a standby mode or normal power mode once power is applied to the device ***and for controlling the initial assignment of a configuration address*** and memory for storing the configuration address ***from the bus upon being enabled by a signal from the circuit after it is activated by a software application into the normal power mode.***
> (emphasis added)

Miner teaches a computer peripheral device (RIU 209, 210) comprising a memory for storing configuration address (col. 11, lines 42-67) and a power level control circuit consisting of standby mode and active mode processors for controlling the power level in the device (Fig 4 and col.11 lines 42-67). The circuit is coupled to the memory which stores the configuration address from a bus when the device enters normal power mode upon being powered up (Fig 4. and Col. 11 lines 42-67). Nothing in Miner discloses that the assignment of configuration address from the bus to the memory is

under the control of the power level control circuit which only enters into the normal power mode when activated by a software application.

In contrast, independent claim 1 includes the limitation of an independent power level control circuit "controlling the initial assignment of a configuration address" when "activated by a software application". As such, the applicant respectfully submits that claim 1 as amended is not anticipated by Miner under 35 U.S.C. §102(e) and respectfully request the withdrawal of the rejection of claim.

Miner teaches a computer system comprising a processor and a plurality of peripheral devices coupled to the processor through at least one bus (Fig. 2) with each device having a power level control circuit for causing the device to be in stand by or normal power mode once power is supplied to the device and the memory stores the configuration address from the bus when the circuit is powered up in the normal power mode (Fig. 2 and col. 11 lines 42-67). Nothing in Miner discloses that the assignment of configuration address from the bus to the memory is under the control of the power level control circuit after entering into the normal power mode when activated by a software application.

In contrast, independent claim 8 includes the limitation that the power level control circuit is "controlling the initial assignment of a configuration address" whereby the memory only stores the specific configuration address after "being enabled by a signal from the circuit after the circuit is activated by a software application into normal power mode." As such, the applicant respectfully submits that claim 8 as amended is

not anticipated by Miner under 35 U.S.C. §102(e) and respectfully request the withdrawal of the rejection of claim.

Claim 9 directly depends on independent claim 8 as amended, thus include the limitation that the power level control circuit is "controlling the initial assignment of a configuration address" whereby the memory only stores the specific configuration address after "being enabled by a signal from the circuit after the circuit is activated by a software application into normal power mode." As such, the applicant respectfully submits that claim 9 is not anticipated by Miner under 35 U.S.C. §102(e) and respectfully request the withdrawal of the rejection of claim.

Claim Rejections - §103

Claims 2-5 and 7 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Miner in view of Michael.

Amended independent claim 1 provides:

> A computer peripheral device comprising:
> a memory for storing a configuration address; and
> an independent power level control circuit for controlling the power level in the device so as to be in a standby mode or normal power mode after power is applied to the device, the circuit being coupled to the memory to ***control an initial assignment of*** configuration address from a bus ***to the memory when the circuit enters the normal power mode after it is activated by a software application.***. (emphasis added).

Independent claim 1 included the limitation where the power level control circuit "controls an initial assignment" of configuration address from a bus to the memory when the circuit enters the normal power mode "after it is activated by a software application."

Miner teaches a computer peripheral device comprising a memory for storing a configuration address coupled to a power level control circuit for controlling the power level in the device so as to be in standby or power-on mode while causing the memory to store the configuration address from a bus when the peripheral device enters a normal power mode. Nothing in Miner suggest that action of writing an address from the bus into the memory is controlled by the circuit which is only activated into normal power mode upon receiving a signal from a software application.

Michael discloses a computer system which would allow a PC host system or other computer system to analyze an I/O address space and automatically assign I/O address to one or more peripheral devices without these devices having to interact or become active in the I/O address space first (Fig. 1 and Col. 2 lines 55-60). Nothing in Michael discloses or teaches a peripheral device containing a memory to store configuration address and a power level control circuit that controls the power level of the device, and upon activation by a software application, controls the assignment of configuration address to the memory. In fact, Michael fails to cure the deficiency of Miner.

It is respectfully submitted that Miner and Michael do not teach or suggest a combination with each other. It would be impermissible hindsight, based on applicant's own disclosure, to combine Miner and Michael.

Applicant respectfully submits that there is no motivation to combine Miner and Michael. The office Action states that "it would have been obvious to one of ordinary skill in the art at the time the invention was made to include once storing a configuration address, retaining that address until the device is reset or power is turned on or off, and

the memory device does not change its stored address when the device is reconfigured as taught by Michael in the system of Miner to save time for address configuration process since the address is retained until the system is powered up again." (Office action, 08/24/04, page 4). Here the Office Action merely states the convenience of integrating the process described by Michael into Miner's system without explaining the specific understanding or technological principle within the knowledge of one skilled in the art would have suggested the combination.

Even if Miner and Michael were somehow combined, the combination would not result in dependent claims 2, 3, and 7. In fact, Michael's system is capable of not resetting the I/O address of the device each time the system is powered up if the register is a non-volatile memory (Col. 6, lines 37-40), such is not the case with the present invention. In particular, the combination would not include the limitation in amended independent claim 1 where the power level control circuit "controls an initial assignment" of configuration address from a bus to the memory when the circuit enters the normal power mode "after it is activated by a software application."

Therefore, applicant respectfully submits that claims 2, 3 and 7 are not unpatentable over Miner in view of Michael. Claims 4 and 5 either directly or indirectly depends on amended independent claim 1 and thus include the limitation of that base claim. As such, Applicant respectfully submits that claims 4 and 5 are also not unpatentable over Miner in view of Michael under 35 U.S.C. §103(a) and respectfully request the withdrawal of the rejection of the claims.

Claim 6 has been rejected under 35 U.S.C. §103(a) as being unpatenable over Miner in view of Michael as applied to claim 5 and further in view of Applicant's Admitted Prior Art (hereinafter AAPA).

The original claim 6 states:

The device defined by claim 5 wherein the circuit is responsive to two addresses once a configuration address is stored.

Claim 6 indirectly depends on independent claim 1, thus includes the limitation where the power level control circuit "controls an initial assignment" of configuration address from a bus to the memory when the circuit enters the normal power mode "after it is activated by a software application." Miner teaches a peripheral device without specifying the initiation and control of address configuration and Michael discloses an automatic assignment of I/O addresses without specifying the address configuration process within a peripheral device, neither cured the limitation that is included in claim 1 as amended. Applicant respectfully submits that Miner and Michael do not teach or suggest a combination with each other.

The office action states that "AAPA teaches peripheral devices which are responsive to two addresses (two addresses are required for operation of the peripheral device in most instances such as for SIO) (page 2, paragraph [0004] and page 6, paragraph [0013]). It would have been obvious to one of ordinary skill in the art to include peripheral devices responsive to two addresses as taught by AAPA in the system of Michael to allow operation of peripheral devices such as SIO." (Office Action, 08/24/04, page 5). Here, the Office Action has mistaken the requirement of having 2

addresses hard coded, as compared to having one address coded and responsive to two addresses, for operation.

Typically two addresses are hard-coded to each peripheral device as a requirement for operation of the device. In this invention, only one address is assigned to the memory from the bus which acts as a starting address, but based on this starting address, it can recognize up to two addresses from the same peripheral device without having to be coded for two addresses. For an example such as SIO which often requires two addresses for operation, it is not necessary to configure two addresses into the memory, simply because the memory has one address, it may be looked upon as an address space for the second address that can be mapped and recognized (page 6, paragraph [0013]).

Claims 10 and 11 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Miner in view of Amin.

Amended independent claim 8 provides:

> A computer system comprising:
> a processor; and
> a plurality of peripheral devices coupled to the processor through at least one bus, each device having an independent power level control circuit for controlling the power level in the device to be in a standby mode or normal power mode once power is applied to the device ***and for controlling the initial assignment of a configuration address*** and memory for storing the configuration address from the bus ***upon being enabled by a signal from the circuit after it is activated by a software application into the normal power mode.***
> (emphasis added)

Miner discloses a computer peripheral device comprising a memory for storing a configuration address coupled to a power level control circuit for controlling the power level in the device so as to be in standby or power-on mode while causing the memory to store the configuration address from a bus when the peripheral device enters a normal power mode. Nothing in Miner suggest that action of writing an address from the bus into the memory is controlled by the circuit which is only activated into normal power mode upon receiving a signal from a software application.

Amin teaches a voltage sequencer in powering up electrical systems requiring multiple voltage levels where the control sequencing logic within the voltage sequencer monitors power sources at the output of a number of power regulators and determines when to enable each of the power regulators (Col. 2, lines 41-45). Nothing in Amin discloses details whereby peripheral devices are powered up sequentially according to the assignment of configuration addresses. Further Amin does not teach the assignment of configuration address from the bus to the memory, which is controlled by the power level control circuit, after being activated into a normal power mode from a standby mode through receiving a signal from a software application. In fact, Amin fails to cure the deficiency of Miner.

Applicant respectfully submits that there is no motivation to combine Miner and Amin. The Office Action stated that "It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement sequentially bring each of the peripheral devices into a normal operating mode as taught by Amin in the system of Miner to avoid potentially damaging power spikes (col. 1, lines 34-41)." (Office Action, 08/24/04, page 5). Here the Office Action merely states the advantage of avoiding

potentially damaging power spikes from Amin and applying that to Miner, without understanding the specific technological principle behind the motivation and rationale in application to the current invention. As described in the application, all peripheral devices are in a standby mode once the general purpose output signals are sent to all device. As the general purpose output signal is de-asserted (device goes into normal power mode) for the first device, an address is written to that peripheral device. Only when the configuration address for the first device is assigned will the next device be activated. (Page 8-9, paragraphs [0020-0021]). Thus, the order in which the devices are activated is controlled by assignment of configuration addresses, and not for the rationale of avoiding potentially damaging power spikes.

As such, applicant respectfully submits that Miner and Amin do not teach or suggest a combination with each other. It would be impermissible hindsight, based on applicant's own disclosure, to combine Miner and Amin.

Even if Miner and Amin were somehow combined, the combination would not result in the limitation of claim 8, where the power level control circuit controls the assignment of configuration address only after being enabled by a signal from the circuit after it is activated by a software application into the normal power mode. Claims 10 and 11 either directly or indirectly depends on amended independent claim 8 and thus include the limitation of the base claim. As such, applicant respectfully submits that claims 10 and 11 are not unpatentable over Miner in view of Amin under 35 U.S.C. §103(a) and respectfully request the withdrawal of the rejection of the claims.

Claims 16 –20 have been rejected under 35 U.S.C. §103(a) as unpatentable over Miner in view of Amin.

Amended claim 16 provides:

> A method for operating a computer system comprising:
> applying power to a plurality of peripheral devices;
> entering a power standby mode in the plurality of peripheral devices;
> sequentially entering a normal power mode from the standby mode for each of the peripheral devices; and
> storing a unique configuration address in each device ***only when initiated by a signal from a power level control circuit, as each circuit enters the normal power mode after activated by a software application.***

Miner teaches a method for operating a computer system comprising: applying power to a plurality of peripheral devices (RIU 209, 210). When the RIU 209, 210 is in the boot-up state, the RIU 209, 210 power up, perform self-diagnostic tests, and registers the address configuration with the network control facility 205 over the upstream channel 215 and primary downstream channel 212. (Col. 11, lines 42-62). After RIU 209, 210 completed their boot-up processing, they enter the standby mode and monitor the secondary downstream channel for until a command is detected. Upon detecting a command from a local interface 411 calling for service, the standby processor 409 will compare command to a limited command set and powered up the 407 active processor and proceed to execute the command if there is a match. (col. 12, lines 1-17). Nothing in Miner teaches that the configuration address is only initiated by a signal from a power level control circuit, as each circuit enters the normal power mode from the standby mode as activated by a software application.

Amin teaches a voltage sequencer in powering up electrical systems requiring multiple voltage levels where the control sequencing logic within the voltage sequencer monitors power sources at the output of a number of power regulators and determines when to enable each of the power regulators (Col. 2, lines 41-45). Nothing in Amin discloses details whereby peripheral devices are powered up sequentially according to the assignment of configuration addresses. Further, Amin does not teach that assignment of configuration address from the bus to the memory, which takes place in the normal power mode within a peripheral device, is controlled by the power level control circuit, and is activated into a normal power mode from a standby mode through receiving a signal from a software application. In fact, Amin fails to cure the deficiency of Miner.

Applicant respectfully submits that there is no motivation to combine Miner and Amin. The Office Action stated that "It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement sequentially entering a normal mode for each peripheral device (col. 1, lines 34-41)." (Office Action, 08/24/04, page 6). Here the Office Action merely states the advantage of avoiding potentially damaging power spikes from Amin and applying that to Miner, without understanding the specific technological principle behind the motivation and rationale in application to the current invention. As described in the application, all peripheral devices are in a standby mode once the general purpose output signals are sent to all device. As the general purpose output signal is deasserted (device goes into normal power mode) for the first device, an address is written to that peripheral device. Only when the configuration address for the first device is assigned will the next device be activated.

(Page 8-9, paragraphs [0020-0021]). Thus, the order in which the devices are activated is controlled by assignment of configuration addresses, but not for the rationale of avoiding potentially damaging power spikes.

As such, applicant respectfully submits that Miner and Amin do not teach or suggest a combination with each other. It would be impermissible hindsight, based on applicant's own disclosure, to combine Miner and Amin.

Even if Miner and Amin were somehow combined, the combination would not result in the limitation of claim 16, where the power level control circuit controls the assignment of configuration address only after being enabled by a signal from the circuit after it is activated by a software application into the normal power mode. Claims 17-20 either directly or indirectly depends on amended independent claim 16 and thus include the limitation of the base claim. As such, applicant respectfully submits that claims 16-20 are not unpatentable over Miner in view of Amin under 35 U.S.C. §103(a) and respectfully request the withdrawl of the rejection of the claims.

Claims 12 – 14 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Miner in view of Henrikson.

Amended independent claim 12 provides:

A computer system comprising:

A processor;

An output unit coupled to the processor; and

A plurality of peripheral devices, ***each controlled by a power level control circuit*** coupled to a power level control line from the output unit, ***signals over each control line causing each circuit to be placed in a standby mode or normal power mode***, each peripheral device having a memory coupled to at least one bus which receives and stores a configuration address from the bus ***in response to the signal***

from the circuit which causes the device to enter its normal power mode upon activation of the circuit by a software application.

Miner teaches a computer system comprising a processor (network control facility 205); an output unit (207) coupled to the processor; and a plurality of peripheral devices (RIUS 209, 210) each being coupled to a primary and a secondary downstream channel (212, 213) with signals over the secondary downstream channel (213) causing each device to be placed in a standby mode or normal operating mode after power is applied to the device (Figs. 2, 3, and 4, col. 11, lines 42 – 67). Each peripheral device having a memory which receives and stores a configuration address from the upstream channel (215) and primary downstream channel (212) in response to a signal from the secondary downstream channel (213) upon powered up, which cause the device to enter a normal operating mode (col. 11, line 42 to col. 12 line 17). Nothing in Miner teaches the assignment of a configuration address from the bus to the memory being controlled by a power level control circuit that is only activated from the power level control line upon activation by a software application.

Amin teaches a voltage sequencer in powering up electrical systems requiring multiple voltage levels where the control sequencing logic within the voltage sequencer monitors power sources at the output of a number of power regulators and determines when to enable each of the power regulators (Col. 2, lines 41-45). Nothing in Amin discloses details whereby peripheral devices are powered up sequentially according to the assignment of configuration addresses. Further, Amin does not teach that the assignment of configuration address from the bus to the memory, which takes place in the normal power mode within a peripheral device, is controlled by the power level

control circuit, and is activated into a normal power mode from a standby mode through receiving a signal from a software application.

Henrikson discloses a system of dynamic system to address devices with a separate control line for each device (abstract). Nothing in Henrikson discloses a peripheral device containing a power level control circuit coupled to a power level control line and a memory coupled to at least one bus where the assignment of a configuration address to the bus is directly controlled by a signal from the circuit after the circuit is activated by a software application. As such, Henrikson does not cure the deficiencies in Miner and Amin.

It is respectfully submitted that Miner and applying Henrikson in the system of Amin do not teach or suggest a combination with each other. It would be impermissible hindsight, based on applicant's own disclosure, to combine Miner, Amin and Henrikson.

Applicant respectfully submits that claim 12 is not unpatentable in view of Miner over Henrikson and Amin under 35 U.S.C. §103(a) and respectfully request the withdrawal of the rejection of the claim. Claims 13 and 14 either directly or indirectly depends on amended claim 12 and thus include the limitation where the assignment of a configuration address from the bus to the memory being controlled by a power level control circuit that is only activated from the power level control line upon activation by a software application. As such applicant respectfully submits that the claims 13 and 14 are also not unpatentable over Miner in view of Henrikson and Amin under 35 U.S.C. §103(a) and respectfully request the withdrawal of the rejection of the claims.

Claim 15 has been rejected under 35 U.S.C. §103(a) as being unpatentable over Miner in view of Henrikson as applied to Claim 12 and further in view of Michael.

Miner teaches a computer system comprising a processor (network control facility 205); an output unit (207) coupled to the processor; and a plurality of peripheral devices (RIUS 209, 210) each being coupled to a primary and a secondary downstream channel (212, 213) with signals over the secondary downstream channel (213) causing each device to be placed in a standby mode or normal operating mode after power is applied to the device (Figs. 2, 3, and 4, col. 11, lines 42 – 67). Each peripheral device having a memory which receives and stores a configuration address from the upstream channel (215) and primary downstream channel (212) in response to a signal from the secondary downstream channel (213) upon powered up, which cause the device to enter a normal operating mode (col. 11, line 42 to col. 12 line 17). Nothing in Miner teaches the assignment of a configuration address from the bus to the memory being controlled by a power level control circuit that is only activated from the power level control line upon activation by a software application.

Henrikson discloses a system of dynamic system to address devices with a separate control line for each device (abstract). Nothing in Henrikson discloses a peripheral device containing a power level control circuit coupled to a power level control line and a memory coupled to at least one bus where the assignment of a configuration address to the bus is directly controlled by a signal from the circuit after the circuit is activated by a software application. As such, Henrikson fails to cure the deficiency of Miner.

Michael teaches storing a configuration address only when first entering the normal operating mode after a reset or after power is turned on or off (retaining the address of the device and configuring the address again each time the system is powered up) (Col. 6, lines 35-40). Furthermore, Michael teaches that the I/O addressing scheme described would automatically generate and assign an I/O address for a device connected to an address and data bus prior to the device becoming active in the I/O address space (Col. 6, lines 41-47). On the contrary, the present invention in teaches that after the power is turned on from the off mode (or upon reset), the peripheral device is in standby mode (page 7, paragraph [0017]) until the assignment of configuration address from the bus to the memory is triggered by a signal from the power level control circuit upon activation of the circuit by a software application through the power level control line. As such, Michael fails to cure the deficiency of Miner and Henrikson.

It is respectfully submitted that Miner, Henrikson and Michael do not teach or suggest a combination with each other. It would be impermissible hindsight, based on applicant's own disclosure, to combine Miner, Henrikson and Michael.

Applicant respectfully submits that there is no motivation to combine Miner, Henrikson, and Michael. The Office Action states that "It would have been obvious to one of ordinary skill in the art at the time the invention was made to store a configuration address only when first entering the normal operating mode after a reset or after power is turned on or off as taught by Michael in the system of Miner and Henrikson to save time for address configuration process since the address is retained until the system is powered up again." (Office Action, 08/24/04, page 8). Here the Office Action merely

states the advantage of substituting Michael's automatic I/O address assignment system into Miner and Henrikson without understanding the specific technological principle behind the motivation and rationale in application to the current invention, which is to take advantage of the power level circuitry inside the peripheral device to control the assignment of configuration address to the memory of the device.

Even if Miner, Henrikson, and Michael are somehow combined, the combination will not result in the limitation of amended independent claim 12 where the assignment of a configuration address from the bus to the memory being controlled by a power level control circuit that is only activated from the power level control line upon activation by a software application. Claim 15 directly depends on amended independent claim 12. Therefore, applicant respectfully submits that claim 15 is not unpatentable over Miner in view of Michael and Henrikson under 35 U.S.C. §103(a) and request the withdrawal of the rejection of the claims.

In conclusion, applicant respectfully submits that in view of the amendments and arguments set forth herein, the applicable rejections have been overcome. If the allowance of these claims could be facilitated by a telephone conference, the Examiner is invited to contact Edwin Taylor at (408) 720-8300. Please charge any shortages and credit any overcharges to our Deposit Account No. 02-2666.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 11/8, 2004

Edwin H. Taylor

Attorney for Applicant
Registration No. 25,129

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, CA 90025-1026
(408) 720-8598